

REMARKS

Claims 1 to 7 and 9 to 15 are pending in the application, of which claims 1 and 9 are independent.¹ Favorable reconsideration and further examination are respectfully requested.

Claims 8 and 16 have been canceled, thereby obviating the objection to the drawings.

Claims 1 to 4, 6, 7, 9 to 12, 14 and 15 were rejected over U.S. Patent No. 5,844,437 (Asazawa); and claims 5, 8, 13 and 16 were rejected over Asazawa in view of U.S. Patent No. 6,559,693 (Tung). As shown above, the independent claims have been amended. Withdrawal of the rejections over the prior art is respectfully requested.

The following features of independent claim 1 have been amended, as shown below

a first switch ~~between~~ connected to the power supply potential terminal and connected to the first shared emitter node, the first switch having a first control terminal that comprises part of the input terminals; and

a second switch ~~between~~ connected to the supply potential terminal and connected to the second shared emitter node, the second switch having a second control terminal that comprises part of the input terminals.

The following features of independent claim 9 have been amended, as shown below

a first switch ~~between~~ connected to a power supply potential terminal and connected to the first emitter node, the first switch having a first control terminal that comprises part of the input terminals; and

a second switch ~~between~~ connected to the supply potential terminal and connected to the second emitter node, the second switch having a second control terminal that comprises part of the input terminals.

An advantage of the foregoing configuration is explained in the specification, as follows:

According to the suggested principle, the two switches which are activated using the differential clock signal are related directly to supply potential from the two emitter nodes.

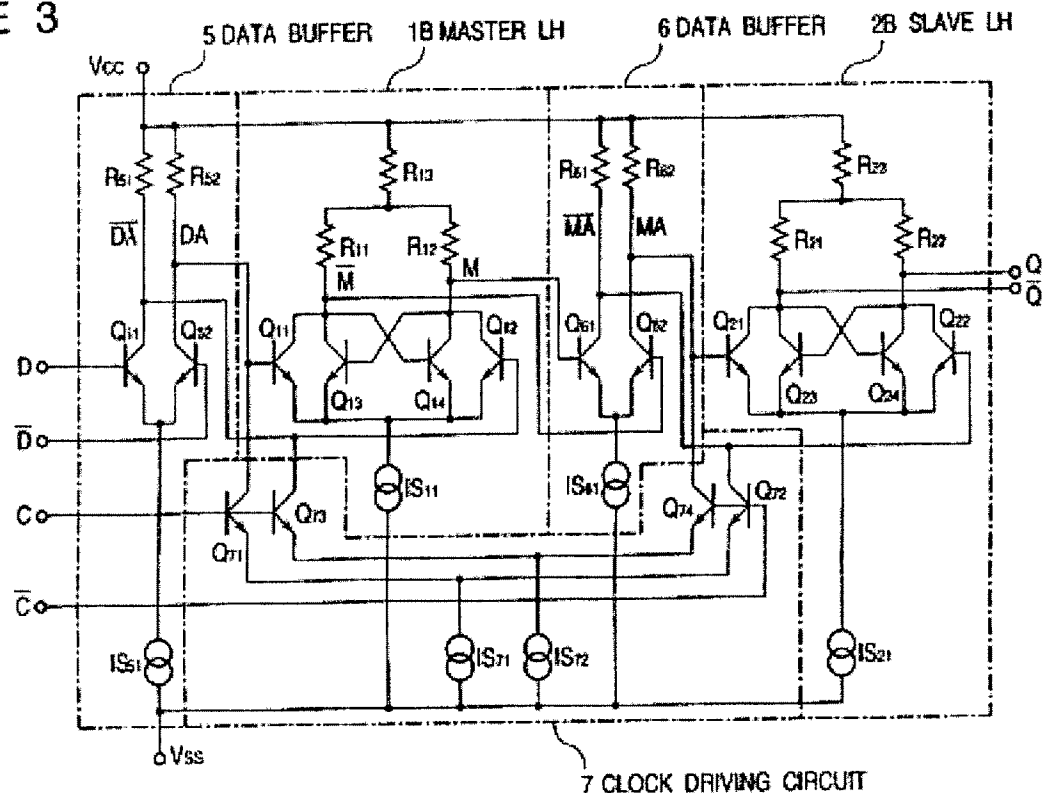
¹ The Examiner is urged to independently confirm this recitation of the pending claims.

Accordingly, the advantage results that only one base-emitter voltage U_{BE} drops out between supply potential terminal and reference potential terminal if the differential amplifier transistors and the switches are implemented in bipolar technology, and therefore the circuit may advantageously be operated using especially low voltage.²

The applied art is not understood to disclose or to suggest the foregoing features and, therefore, is also not believed to achieve the foregoing advantage.

In this regard, the Office Action cites Fig. 3 (below) of Asazawa for its alleged disclosure of a flip flop circuit arrangement in accordance with claim 1.

FIGURE 3



² Specification, page 3, lines 1 to 12

In particular, the Office Action equates Q_{71} to the claims' first switch, and Q_{72} to the claims' second switch.³ However, as is clear from Fig. 3 above, Q_{71} and Q_{72} are not connected as now required by claims 1 and 9. That is, Q_{71} is not connected to the power supply potential terminal and connected to the first shared emitter node; and Q_{72} is not connected to the supply potential terminal and connected to the second shared emitter node.⁴ Rather, there is a resistor R_{52} between Q_{71} and V_{CC} ; and there is a resistor R_{62} between Q_{71} and V_{CC} . Furthermore, Q_{71} is not connected to the first shared emitter node, which is identified in the Office Action as "emitters of Q_{11} - Q_{14} "; and Q_{72} is not connected to the second shared emitter node, which is identified in the Office Action as "emitters of Q_{21} - Q_{24} ".⁵ Rather, as shown in Fig. 3 above, Q_{71} is connected, not to a shared emitter node, but rather to a current source IS_{71} ; and Q_{72} is connected, not to a shared emitter node, but rather to a current source IS_{72} .

We note that page 4 of the Office Action states that the switches and emitters are commonly connected to V_{SS} . While this may be true, the claims now require connection between the switches and the shared emitter nodes. This is clearly the case in Asazawa.

Tung, which was cited for its disclosure of implementing transistors in MOS technology, is not understood to remedy the foregoing deficiencies of Asazawa vis-à-vis claims 1 and 9. Accordingly, claims 1 and 9 are believed to be patentable.

Each of the dependent claims is also believed to define patentable features of the invention. Each dependent claim partakes of the novelty of its corresponding independent claim and, as such, has not been addressed specifically herein.

³ Office Action, page 3, 4 and 6, 7

⁴ Claim 9 does not use the word "shared"; however, the connections are clear from the claim.

⁵ Office Action, page 3

It is believed that all of the pending claims have been addressed. However, the absence of a reply to a specific rejection, issue or comment does not signify agreement with or concession of that rejection, issue or comment. In addition, because the arguments made above may not be exhaustive, there may be reasons for patentability of any or all pending claims (or other claims) that have not been expressed. Finally, nothing in this paper should be construed as an intent to concede any issue with regard to any claim, except as specifically stated in this paper, and the amendment of any claim does not necessarily signify concession of unpatentability of the claim prior to its amendment.

In view of the foregoing amendments and remarks, we respectfully submit that the application is in condition for allowance, and such action is respectfully requested at the Examiner's earliest convenience.

The undersigned attorney can be reached at the address shown below. All telephone calls should be directed to the undersigned at 617-521-7896.

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Please apply any fees or credits due in this case, which have not already been covered by check, to Deposit Account 06-1050 referencing Attorney Docket No. 14603-016US1.

Respectfully submitted,

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